Application No. 10/734,420
Amendment dated July 21, 2006
Office Action mail date: April 27, 2006

REMARKS/ARGUMENTS

Applicants thank the Examiner for the courtesies extended during the interview held on June 6, 2006, in which the claims of the present application and one of the prior art references USP 6,681,359 (Au) were discussed. As the Examiner indicated in the Interview Summary Record dated June 12, 2006, no agreement was reached concerning the claims.

In the Office Action, the Examiner rejected claims 1-4, 7-9, 13-19, and 22-24 under 35 U.S.C. §102(e) as anticipated by Au. The Examiner also rejected claims 5, 10, 11-12, 20, and 25-27 under 35 U.S.C. §103(a) as unpatentable over Au in view of USP 6,370,661 (Miner). The Examiner also rejected claims 6 and 21 under 35 U.S.C. § 103(a) as unpatentable over Au and further in view of USP 7,010,736 (Teh). Applicants respectfully traverse these rejections, and request reconsideration and allowance of the claims in view of the following arguments.

The present invention relates to a memory testing method and system in which memory testing is conducted at the operating frequency of the memory until an error is identified. By testing at the memory operating frequency, as Applicants describe, errors which can occur at otherwise more rapid speeds can be identified. If a failed memory location is identified, the location information for that failure is clocked out to a memory tester at a lower, tester frequency.

Thus, according to the present invention, a test of memory is carried out at two speeds. Memory testing is initiated at the memory operating frequency. If no errors are detected, the test is completed at that frequency. If an error is detected, the test continues at the lower, tester frequency to clock out the error information. Testing is then resumed at the higher memory operating frequency.

In contrast to the present invention, in which memory testing is carried out at two different frequencies in a given test, the Au reference teaches carrying out memory testing at two different frequencies for two different tests, in two different modes of operation. Au describes a non-debug mode of operation in which a memory is tested at the memory operating frequency, and errors are counted. At the end of the test, the count is output. This test does not identify errors by memory location.

Au also describes a debug mode of operation, in which memory testing is carried out at a lower frequency (col. 3, lines 41-43). In this lower speed test, the location of all failing memory cells is returned at the end (*Id.*)

Au also describes testing as preferably beginning in a faster, non-debug mode (col. 8, lines 56-58). Testing in this mode is performed at the full operational speed of the memory, and results in a simple pass/fail verdict, together with a failure count (col. 8, lines 59-61).

At col. 9, lines 34-43, Au describes synchronization of a higher-speed clock BIST_CLK to a lower-speed clock TCK in both non-debug and debug modes. This description appears inconsistent with the stated summary of the invention quoted earlier, in which full testing is done at a slower speed in Au, and also appears inconsistent with the description of Fig. 5 of Au depicting the debug mode, at col. 10, lines 30-51.

In order for a prior art reference to anticipate a claim, it must disclose, expressly or under principles of inherency, all of the claimed limitations. Applicants respectfully submit that Au fails to anticipate, or render obvious the claims of the present application because Au does not disclose or suggest performing a memory test at two different frequencies. Instead, Au suggests carrying out two different tests, one at a first, higher frequency simply to count errors, followed

by a second test at a second, lower frequency to identify failure locations. Thus, Au fails to teach or suggest the features of independent claims 1, 13, or 16.

Independent claim 1 (which has claim 7 combined into it, claim 7 now having been cancelled) recites a memory testing system comprising a first memory tester which detects failed location information at a first frequency, and a second memory tester which receives the failed location information at a second frequency, wherein the first frequency is higher than the second frequency. Independent claim 13 recites a memory testing method in which failed location information is transferred from a memory to a first memory tester at a first frequency, and from the first memory tester to a second memory tester at a second frequency that is lower than the first frequency. Independent claim 16 (which has claim 22 combined into it, claim 22, now having been cancelled) recites a memory testing system comprising means for detecting failed location information from a memory at a first frequency, and means for receiving the failed location information at a second frequency, wherein the first frequency is higher than the second frequency. Therefore, Applicants submit that claims 1-6, 8-21, and 23-27 in the subject application are patentable.

Neither Miner nor Teh, which the Examiner has applied against dependent claims, remedy any of the deficiencies of Au. Therefore, pursuant to the foregoing discussion, Applicants respectfully request that the Examiner reconsider and withdraw these rejections.

Request for Allowance

It is believed that this Amendment places the application in condition for allowance, and early favorable consideration of this Amendment is earnestly solicited.

Atty. Docket No. MP0263 (13298/3)
PATENT APPLICATION

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If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the telephone number listed below.

The Office is hereby authorized to charge any fees, or credit any overpayments, to Deposit Account No. **11-0600.**

Respectfully submitted,
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Dated: July 21, 2006

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I hereby certify that this paper is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: MAIL STOP AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 21, 2006.

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